8-bit shift register with 2:1 mux-in, latched “B” inputs, and serial out

74F835

FEATURES

- Specifically designed for Video applications
- Combines the 74F373, two 74F157s, and the 74F166 functions in one package
- Interleaved loading with 2:1 mux
- Dual 8-bit parallel inputs
- Transparent latch on all “B” inputs
- Guaranteed serial shift frequency to 100MHz
- Expandable to 16-bits or more with serial input

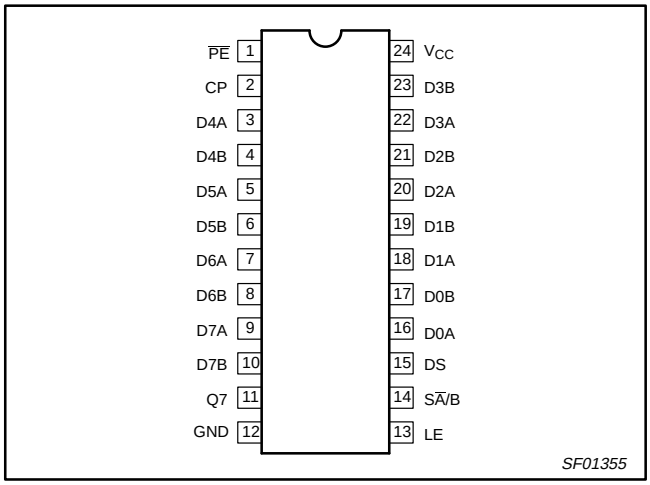
DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the “B” inputs connected to an octal latch.

This 24-pin part is specifically designed for video bit shifting, where interleaved loading is desired and parts count is critical. It is useful in any design where a 2:1 mux input with a transparent latch is needed.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	150MHz	45mA

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24-pin plastic Slim DIP (300 mil)	N74F835N	SOT222-1
24-pin plastic SOL	N74F835D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0A – D7A	Parallel data inputs	1.0/1.0	20µA/0.6mA
D0B – D7B	Latched Parallel data inputs	1.0/1.0	20µA/0.6mA
DS	Serial data input	1.0/1.0	20µA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
SA/B	Mux Select	1.0/1.0	20µA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20µA/0.6mA
PE	Parallel Enable input	1.0/1.0	20µA/0.6mA
Q7	Output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

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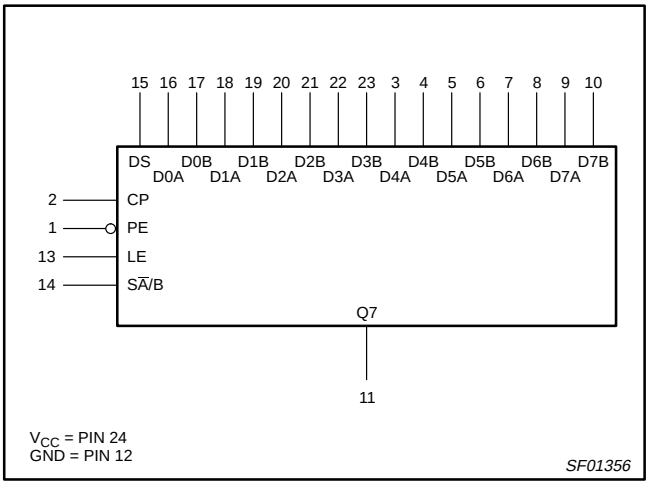
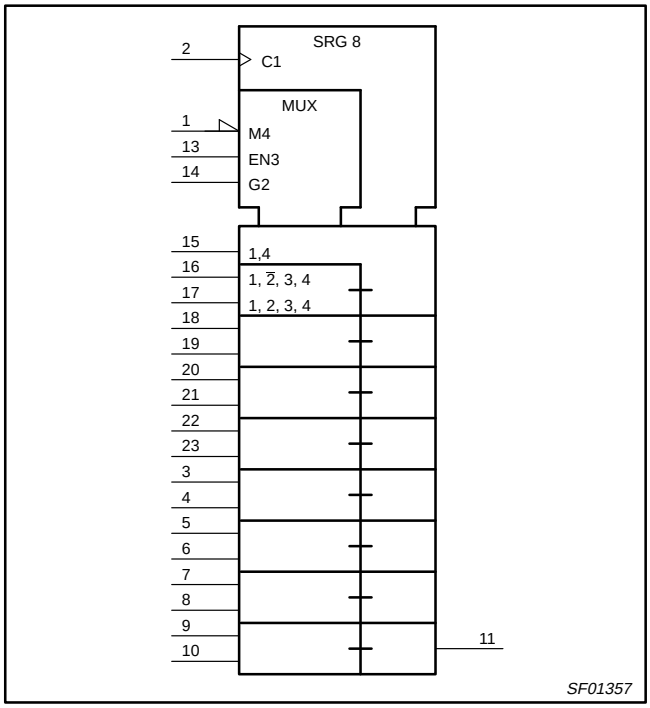
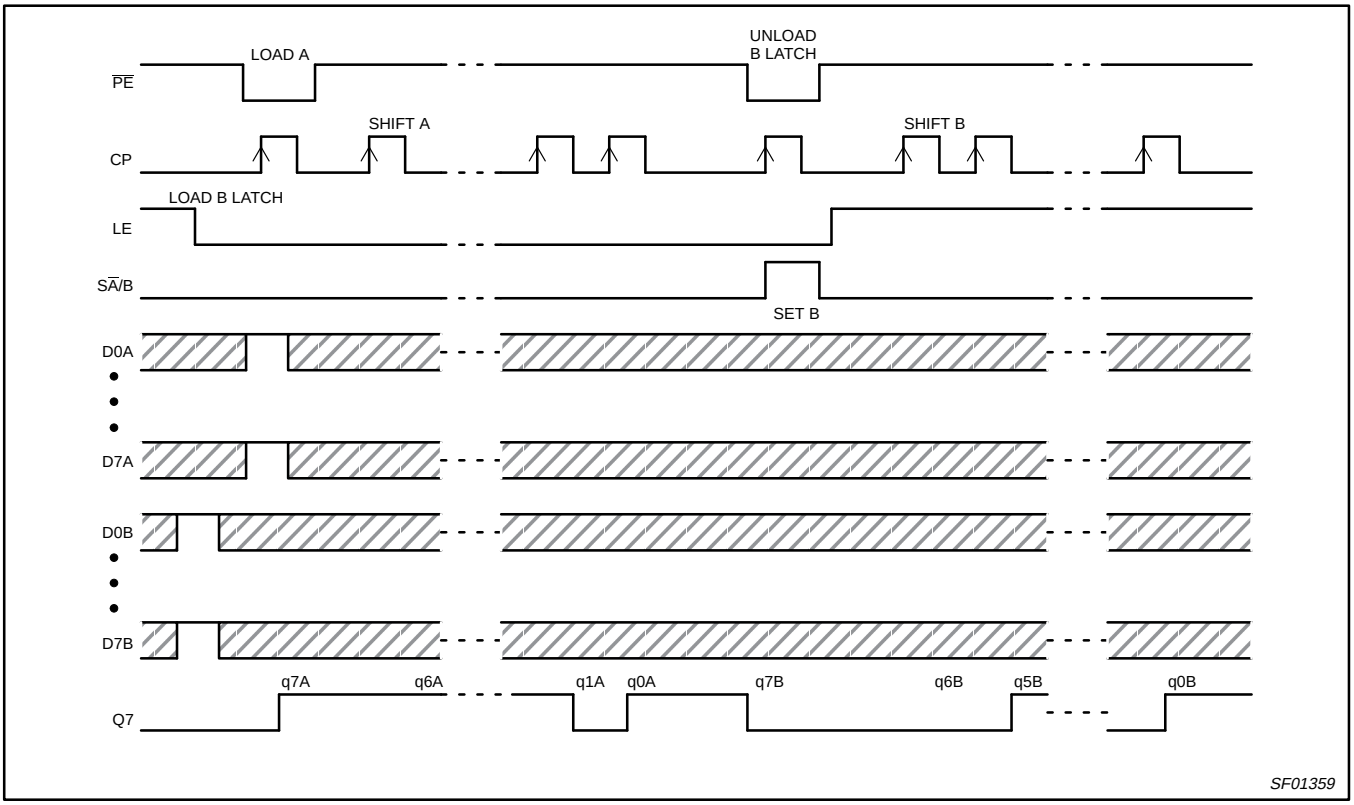
LOGIC SYMBOL



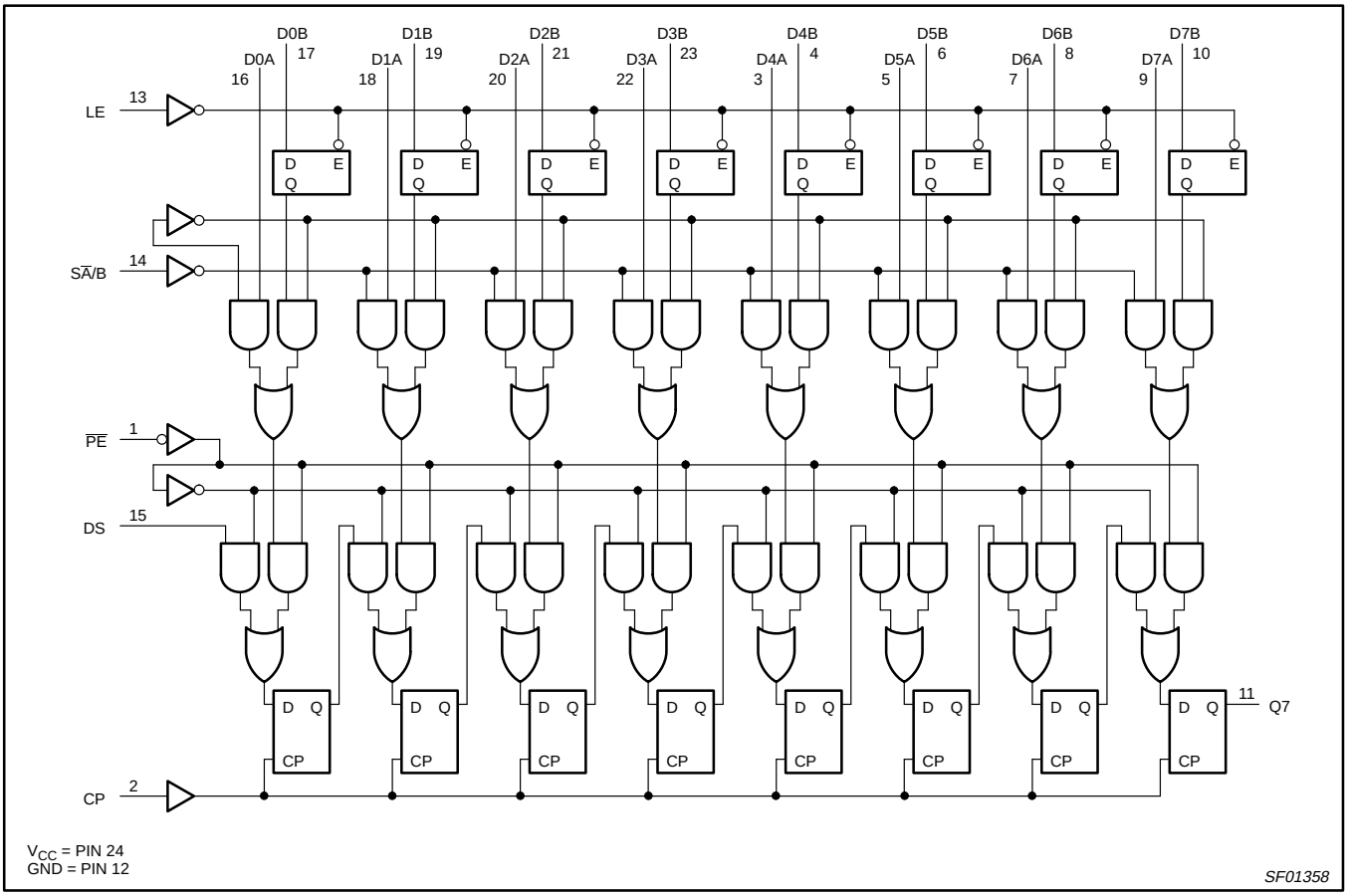
IEC/IEEE SYMBOL



TYPICAL TIMING DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS							INTERNAL			OUTPUT
								B LATCH	SERIAL REGISTER		
	$\overline{PE}$	CP	LE	SA/B	DnA	DnB	DS		Q0	Q1–6	Q7
Parallel load A data	L	↑	X	L	h l	X X	X X	X X	H L	H L	H L
Latch B data	X	X	L	X	X X	h l	X X	H L	X X	X X	X X
Parallel load B data (from Latch)	L	↑	L	H	X X	X X	X X	h l	H L	H L	H L
Parallel load B data (Transparent Mode)	L	↑	H	H	X X	h l	X X	h l	H L	H L	H L
Serial Shift	H	↑	X	X	X X	X X	h l	X X	H L	qn–1 qn–1	q6 q6

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don’t care
qn = Lower case letters indicate the state of the referenced flop cell one cycle prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10% V_{CC}	2.5			V
			±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH}L= MAX	±10% V_{CC}		0.30	0.50	V
			±5% V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			45	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V. T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

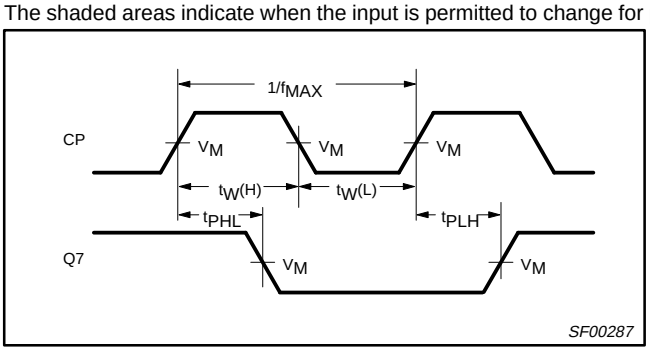
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	130	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q7 (Load)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q7 (Shift)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns

AC SETUP REQUIREMENTS

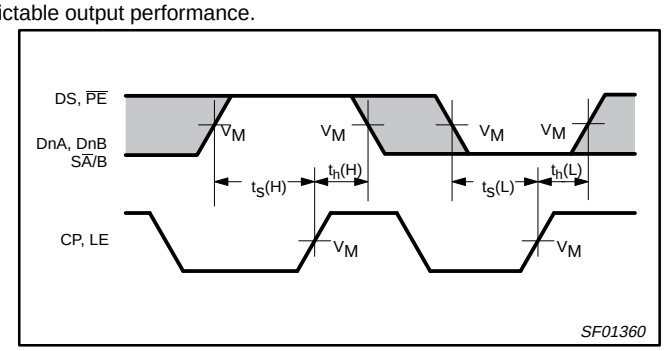
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time DnA or DnB to CP	Waveform 2	3.5 3.5			3.5 3.5		ns
t_h(H) t_h(L)	Hold time DnA or DnB to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
t_s(H) t_s(L)	Setup time DS to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
t_h(H) t_h(L)	Hold time DS to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
t_s(H) t_s(L)	Setup time $\overline{PE}$ to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
t_h(H) t_h(L)	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t_s(H) t_s(L)	Setup time DnB to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
t_h(H) t_h(L)	Hold time DnB to LE	Waveform 2	3.0 3.0			4.0 4.0		ns
t_s(H) t_s(L)	Setup time S$\overline{A}$/B to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
t_h(H) t_h(L)	Hold time S$\overline{A}$/B to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	clock pulse width, High or Low	Waveform 1	4.5 4.5			5.5 5.0		ns
t_w(H)	Latch Enable pulse width, High	Waveform 1	4.5			5.0		ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

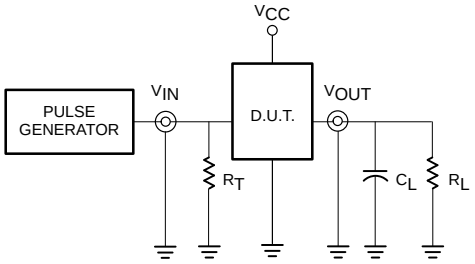


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

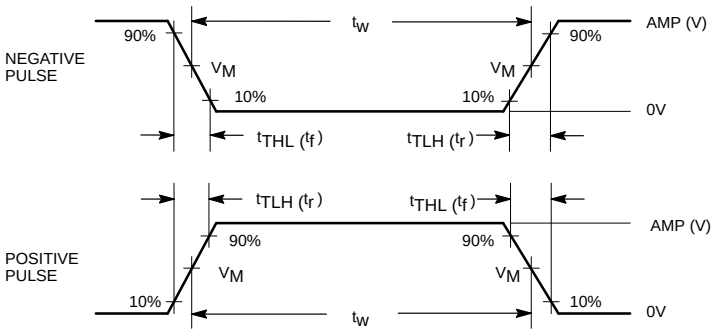


Waveform 2. Data and Select Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006